Analysis of Packaging Effects and Optimization in Inductively Degenerated Common-Emitter Low-Noise Amplifiers

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***Abstract*—The effects of packaging on the performance of inductively degenerated common-emitter low-noise amplifiers (LNAs) are examined and the equations describing the input impedance, transconductance, voltage gain, and noise figure of the packaged amplifier are derived. From the equations, several guidelines for the LNA design are obtained and a systematic approach for the LNA design can be derived. Furthermore, by applying the formulas, the performance of the amplifier can be readily estimated and optimized in the very early stage of the circuit design, immediately as the process data is available. The measurement results of the implemented 0.35-μm SiGe RF front-end with an inductively degenerated common-emitter LNA at 1.575 GHz agree well with calculations and simulations.**

***Index Terms*—BiCMOS, low-noise amplifier (LNA), packaging effects, RF.**

I. Introduction

In MASS product applications, the integrated circuits are almost always mounted in a package. At RF frequencies, the package parasitics can have a significant effect to the circuit performance and they cannot be neglected. Therefore, the models for the package parasitics are vital to predict the circuit performance. For the circuit simulations, accurate models for the parasitics are preferred, but also analytical models are useful to give insight how the circuit properties are modified by the parasitics.

In typical direct conversion or low-IF receivers with on-chip voltage-controlled oscillators (VCOs) [1]–[3], the only RF off-chip interface is the low-noise amplifier (LNA) input. Thus, the package parasitics have an effect on the receiver performance only via the LNA input, assuming that a balanced LNA topology is used. Nonideal ground and supply pins have a significant effect only on the common-mode signals. In this study, a balanced LNA is used to reject the interference from the substrate or supply.

In this paper, the effects of packaging on the performance of inductively degenerated common-emitter LNAs, shown in Fig. 1(a), are studied and the selection of the LNA input-impedance level is highlighted. Although most of the reported wireless receivers use this LNA architecture [3]–[6], the effects of the package parasitics are for simplicity usually neglected in the analysis. The input impedance of the MOS version of circuit shown in Fig. 1(a) with pad or package parasitics has been analyzed in [7], [8], and [13], but analytical expressions for the input stage transconductance, noise figure (NF), or voltage gain have not been given. In [9], the NF and gain of the MOS LNA with parasitics are also analyzed, but in the case of nonperfect impedance match at the LNA input. In mass product applications, this is not practical since the LNA must meet its input-impedance-matching requirements also in the presence of process and temperature variations. If the nominal LNA S_{11} is designed to be only approximately -10 dB, the amplifier will most probably fail to meet its matching specifications in the process corners. For this reason, the equations given in this paper assume a perfect match at the LNA input. Moreover, the derived formulas give insight into the factors affecting the performance of the packaged amplifier and, therefore, for the whole RF front-end. For example, the NF of the LNA sets the minimum theoretically achievable NF for the whole front-end. On the other hand, since the front-end linearity is typically dominated by the mixer linearity, the linearity of the LNA is not considered here.

Section II reviews the performance of inductively degenerated common-emitter amplifier in the absence of package parasitics and Section III shows how the performance is affected by the parasitics. The actual implementation based on the derived results is presented in Section IV. Finally, experimental results are discussed.

II. LNA in Absence of Package Parasitics

The effect of packaging on LNA performance can be analyzed by considering the circuit shown in Fig. 1. Only the single-ended equivalent circuit is shown, but the results to be derived also apply to the balanced configuration. The cascode transistor Q_2 lowers the local oscillator (LO) leakage produced by the following mixer and improves the stability of the circuit. The package parasitics are modeled with two circuit elements, i.e., C_p and $L_{\rm bw}$. In Fig. 1, $L_b' = L_b + L_{\rm bw}$, where L_b is an external inductor and $L_{\rm bw}$ is the sum of the self-inductance of the bondwire and the inductance due to the mutual inductance between the adjacent bondwires. An external base inductance L_b is typically needed to provide the series resonance for the input-impedance matching. C_p is the sum of the Miller capacitance of the input device, pad, and package capacitance. The model for the parasitics can be made relatively accurate provided that the adjacent pins of RF signals are grounded or otherwise properly terminated.

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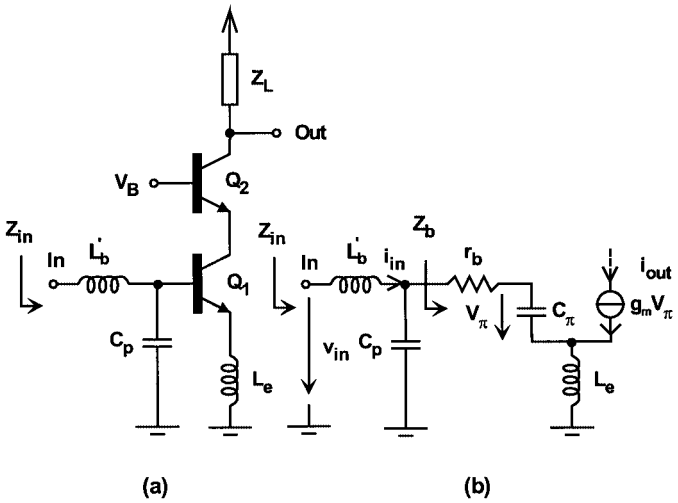

Fig. 1. (a) Single-ended equivalent circuit of the LNA. (b) Its input stage small-signal model.

Consider first an LNA in the absence of package parasitics, i.e., $C_p = 0$ and $L_b' = L_b$. At the resonance frequency

$$f_0 = \frac{1}{2\pi\sqrt{(L_b + L_e)C_\pi}} \tag{1}$$

the input impedance of the LNA can be approximated as

$$Z_{\text{in}} = \frac{g_m L_e}{C_\pi} + r_b \tag{2}$$

where L_e is the emitter inductance, C_π is the base–emitter capacitance of Q_1, g_m is the transconductance of Q_1, and r_b is the base resistance of Q_1.

At the resonance frequency, the transconductance of the input stage is given as

$$G_m = \left|\frac{i_{\text{out}}}{v_{\text{in}}}\right| = \left|\frac{g_m v_\pi}{v_{\text{in}}}\right| = \frac{g_m}{\omega_0(g_m L_e + r_b C_\pi)} \approx \frac{1}{\omega_0 L_e} \tag{3}$$

since, by a proper design, $(g_m Le/C_\pi) \gg r_b$. Therefore, G_m of the LNA at ω_0 is relatively independent of the device g_m itself. The LNA voltage gain at ω_0 is now simply given as

$$A_v = |G_m Z_L(j\omega_0)| \approx \frac{|Z_L(j\omega_0)|}{\omega_0 L_e} \tag{4}$$

where $Z_L(j\omega_0)$ is the load impedance of the LNA at ω_0.

The NF of the unpackaged LNA at the resonance frequency can be estimated by analyzing the circuit shown in Fig. 2 [10] ($C_p = 0$ and $L_b' = L_b$). If the noise contributions of the cascode transistors are neglected and perfect input-impedance matching ($Z_{\text{in}} = R_s$) is assumed, the NF can be written as [11]

$$\text{NF} = 1 + \frac{R_{lb}}{R_s} + \frac{r_b}{R_s} + \frac{g_m R_s}{2\beta_0} + \frac{1}{2g_m R_s \beta_0}\left(\frac{\omega_T}{\omega_0}\right)^2 + \frac{g_m R_s}{2}\left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{4R_s}{R_L}\left(\frac{\omega_0}{\omega_T}\right)^2 \tag{5}$$

where R_{lb} is the series resistance of the base inductor L_b, β_0 is the low-frequency current gain of Q_1, R_s is the output resistance of preceding stage, $\omega_T \approx g_m/C_\pi$ is the unity-current gain angular frequency of Q_1, and R_L is the equivalent parallel load resistance of the LNA.

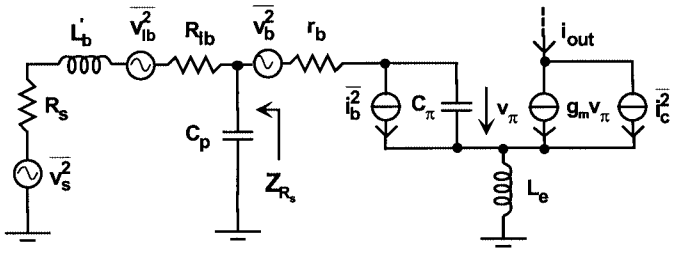

Fig. 2. Circuit model for input stage noise analysis.

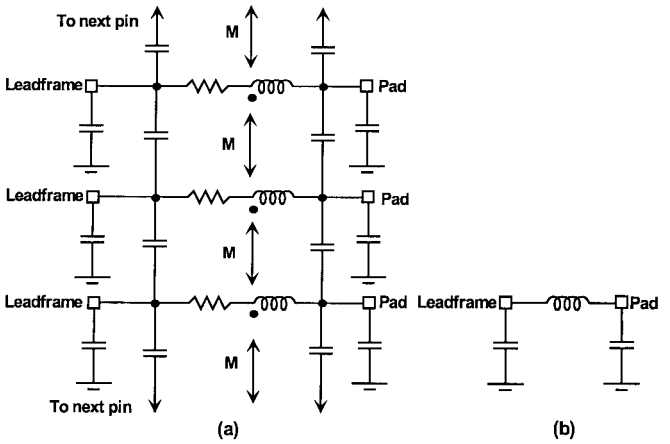

Fig. 3. (a) Detailed and (b) reduced package models for LNA input signal pins.

III. LNA With Package Parasitics

The model for the package parasitics used in hand calculations (Fig. 1) uses only two additional circuit elements C_p and L_{bw}. Nevertheless, it will still give us a clear and accurate insight as to how the properties of the LNA are modified by the package. In simulations, however, a detailed model shown in Fig. 3(a) is used.

The differential input signal pins of the LNA are selected so that the adjacent pins are ground pins. Therefore, each coupling capacitance shown in Fig. 3(a) between the signal pin and adjacent ground pin presents a parallel capacitance between the signal pin and ground. The resistance in series with the bondwire is negligible in practice. Thus, the package model for the both LNA input signal pins is reduced to the π-network shown in Fig. 3(b). Finally, for hand calculation purposes, all the parallel capacitances can be reduced to the pad side without significant error in results.

The effect of packaging on the LNA input-impedance matching can be analyzed by using a parallel-series transformation technique, as shown in Fig. 4 [12], [13]. The transformation is not valid in general, but near resonance, the equivalence is reasonable [14]. In this case, the base inductance L_b' needed to series resonate the LNA input impedance at the frequency of interest is given as

$$L_b' \approx \frac{1}{\omega_0^2(C_p + C_\pi)}. \tag{6}$$

Therefore, compared to the unpackaged LNA, the packaged amplifier requires smaller base inductance to series resonate the

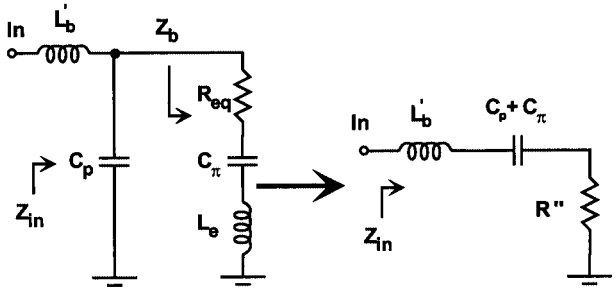

Fig. 4. LNA input impedance in the presence of package parasitics is analyzed by using parallel-series transformation technique.

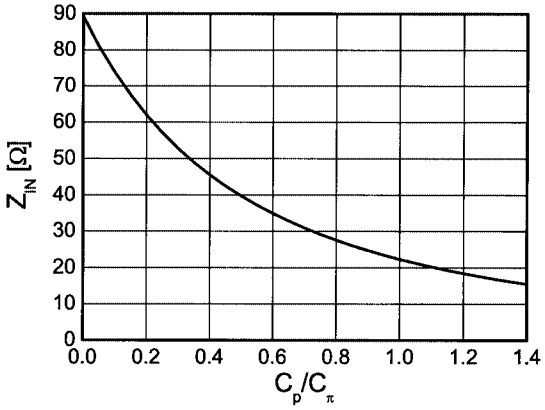

Fig. 5. Effect of package parasitic capacitance C_p on single-ended LNA input impedance.

input impedance with given frequency of operation and device size (C_π). The resulted real input impedance at ω_0 is given as

$$Z_{\text{in}} = R'' \approx k^2 \cdot R_{\text{eq}} \tag{7}$$

where

$$k = \frac{C_\pi}{C_p + C_\pi} \tag{8}$$

and

$$R_{\text{eq}} = \frac{g_m Le}{C_\pi} + r_b. \tag{9}$$

Thus, due to the parasitic capacitance C_p at the transistor base, the input impedance comes down by a factor of k^2 $(k \leq 1)$ compared to the unpackaged LNA with a given size of L_e, collector current (g_m), and device size (C_π, r_b).

The effect of C_p on the single-ended LNA input impedance Z_{in} at the resonance is illustrated graphically in Fig. 5. The component values used are $I_c = 1.1$ mA, $L_e = 1.1$ nH, $C_\pi = 575$ fF, and $r_b = 5\ \Omega$ giving $R_{\text{eq}} \approx 89\ \Omega$. The values are taken from the designed LNA.

The transconductance of the input stage is also found with the help of the parallel-series transformation steps, as illustrated in

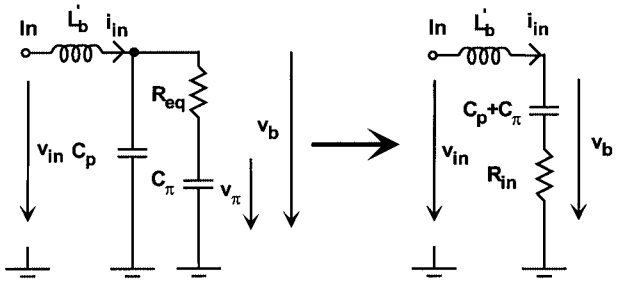

Fig. 6. Analysis of input stage transconductance G_m.

Fig. 6. By applying a straightforward circuit analysis, the magnitude of the input stage output current i_{out} can be approximated as

$$\begin{aligned} |i_{\text{out}}| &= g_m |v_\pi| \\ &\approx \frac{g_m |v_b|}{\sqrt{1 + \omega_0^2 C_\pi^2 R_{\text{eq}}^2}} \\ &\approx \frac{g_m |v_{\text{in}}|}{\omega_0 (C_p + C_\pi) R_{\text{in}} \sqrt{1 + \omega_0^2 C_\pi^2 R_{\text{eq}}^2}} \\ &\approx \frac{g_m |v_{\text{in}}|}{k \omega_0 C_\pi R_{\text{eq}} \sqrt{1 + \omega_0^2 C_\pi^2 R_{\text{eq}}^2}} \end{aligned} \tag{10}$$

where R_{in} and R_{eq} are given in (7) and (9), respectively. Thus, the input stage transconductance at ω_0 is

$$G_m = \left| \frac{i_{\text{out}}}{v_{\text{in}}} \right| \approx \frac{g_m}{k \omega_0 C_\pi R_{\text{eq}} \sqrt{1 + \omega_0^2 C_\pi^2 R_{\text{eq}}^2}} \approx \frac{1}{k} \cdot \frac{1}{\omega_0 L_e} \tag{11}$$

which is seen to be approximately $1/k$ times larger than G_m without the packaging with a given size of L_e. Moreover, again, the LNA input stage transconductance at the resonance frequency is relatively independent of the device g_m.

The NF of the packaged LNA can be computed by analyzing the circuit shown in Fig. 2 $((C_p \neq 0))$. First, however, the impedance Z_{R_s} looking into the generator is transformed to the series impedance at ω_0. By carrying out the analysis, it can be shown that the LNA NF in the presence of package parasitics at ω_0 is given by

$$\begin{aligned} \text{NF} = 1 + \frac{R_{lb}}{R_s} + \frac{r_b k^2}{R_s} + \frac{g_m R_s}{2\beta_0 k^2} + \frac{k^2}{2 g_m R_s \beta_0} \left(\frac{\omega_T}{\omega_0} \right)^2 \\ + \frac{g_m R_s}{2k^2} \left(\frac{\omega_0}{\omega_T} \right)^2 + \frac{4R_s}{R_L k^2} \left(\frac{\omega_0}{\omega_T} \right)^2. \end{aligned} \tag{12}$$

It is seen that, excluding the term R_{lb}/R_s, the equation for the NF of the packaged LNA is obtained from the unpackaged case [see (5)] by simply replacing the generator resistance R_s with R_s/k^2.

From the equations derived, several guidelines for the packaged LNA design can be given. These general guidelines are actually very similar for the unpackaged amplifier. First, from (12), it is seen that the transistor size has to be selected to be sufficiently large in order to ensure that the contribution of the base resistance r_b to the NF is negligible. The selection of the input

device size also fixes largely C_π and, therefore, factor k given by (8). Thus, according to (7), the real part of the input impedance can be adjusted by tuning the bias current (g_m) or the emitter inductance L_e. As the size of L_e is selected, the voltage gain can still be adjusted by tuning the load impedance Z_L. The equivalent parallel load resistance R_L has to also be selected large enough to minimize its noise contribution. Moreover, as the contribution of the series resistance R_b of the base inductor L_b is seen directly on the NF, L_b is usually realized as a high-quality off-chip inductor. Finally, as g_m and ω_T both depend on the bias current I_c, computer optimization is needed to minimize the NF and to obtain an optimum performance as a whole.

Now the performance of unpackaged and packaged balanced LNAs consuming an equal amount of power and using an equal size of the active device, emitter inductance L_e, and load resistance R_L will be compared in terms of transducer power gain and NF at the resonance frequency. It should be noticed that g_m and C_π of the input device in both cases are also equal. Only the different sizes of external base inductors are used to tune the resonance at the desired frequency. Moreover, it is assumed that an external lossless $1{:}T$ impedance transformer is used to convert the single-ended RF signal to differential for the LNA. Assuming perfect input-impedance match, the impedance transformation ratio T is related to the single-ended LNA input impedance $Z_{\rm in}$ and source resistance R_s (typically 50 Ω) as

$$T = \frac{2Z_{\rm in}}{R_s}. \tag{13}$$

According to (13), the impedance transformation ratio T required in the packaged case is k^2 times smaller than the ratio needed in the unpackaged case. The available power from the source V_s is defined as

$$P_{\rm avs} = \frac{V_s^2}{4R_s}. \tag{14}$$

The magnitude of the LNA input stage output current at the resonance frequency can then be expressed as

$$|i_{\rm out}| = G_m \frac{|v_{\rm in}|}{2} = \frac{G_m}{2}\sqrt{T}\frac{|v_s|}{2} \tag{15}$$

and the transducer power gain can be written as

$$G = \frac{P_L}{P_{\rm avs}} = \frac{2R_L|i_{\rm out}|^2}{P_{\rm avs}} = \frac{R_L R_s G_m^2 T}{2}. \tag{16}$$

The transducer power gains of the unpackaged and packaged LNAs can then be expressed as

$$G_u = \frac{R_L R_s G_{m,u}^2 T_u}{2} = \frac{R_L R_s G_{m,u}^2}{2}\frac{2Z_{{\rm in},u}}{R_s} = R_L Z_{{\rm in},u} G_{m,u}^2 \tag{17}$$

and

$$\begin{aligned} G_p =& \frac{R_L R_s G_{m,p}^2 T_p}{2} \\ =& \frac{R_L R_s G_{m,p}^2}{2}\frac{2Z_{{\rm in},p}}{R_s} \\ \approx& R_L k^2 Z_{{\rm in},u}\frac{G_{m,u}^2}{k^2} \\ =& G_u \end{aligned} \tag{18}$$

where (7) and (11) have been applied and the subscripts u and p denote the unpackaged and packaged cases, respectively. According to (18), the transducer power gains in both LNA cases are approximately equal.

In the unpacked case, the NF of the LNA is given by (5) and the amplifier is matched to the (single-ended) impedance $R_{s,u} = (g_m L_e/C_\pi + r_b)$ looking into the source. Correspondingly, the NF of the packaged LNA is given by (12) and the amplifier is matched to the impedance $R_{s,p} = k^2(g_m L_e/C_\pi + r_b) = k^2 R_{s,u}$ looking into the source. Thus, by replacing $R_{s,p}$ in (12) by $k^2 R_{s,u}$ and neglecting term R_b/R_s, we get exactly (5). Therefore, the NFs in both of the LNA cases are approximately equal.

Since the transducer power gains and NFs of the unpackaged and packaged balanced LNAs consuming an equal amount of power and using an equal size of the active device, emitter inductance L_e, and load resistance R_L are equal, it is concluded that the packaging does not worsen the properties of the inductively degenerated amplifier. In the packaged amplifier, only smaller base inductance is needed to series resonate the input impedance, and the transformer with lower impedance transformation ratio T is required to transform the balanced input impedance to single ended and to match the input impedance to the output resistance of the preceding stage or the source resistance R_s (typically 50 Ω).

In this design, C_π and C_p are within the same order of magnitude, i.e., $C_\pi \approx C_p$ or $k^2 \approx 0.25$. With typical component values $I_c = 1.1$ mA, $L_e = 1.1$ nH, $C_\pi = 575$ fF, and $r_b = 5\ \Omega$ taken from the designed LNA, (7) predicts $Z_{\rm in} \approx 21.4\ \Omega$. Thus, due to the parasitic capacitance C_p, the resulted single-ended LNA input impedance is in the order of a few tens of ohms instead of the traditionally used 50 Ω. For this reason, the LNA input impedance at the frequency of operation was selected to be approximately a 50-Ω differential instead of a typical 100-Ω differential. This is also possible in the practical point-of-view since low-loss external baluns or preselection filters are available for an impedance transformation ratio of 1 : 1. This corresponds to the differential impedance level of 50 Ω at the secondary port, assuming that the primary port is terminated with 50 Ω.

It should be noticed that, in the packaged case, it is actually difficult to design the LNA input impedance to be much larger than a few tens of ohms (i.e., traditional 50 Ω) with adequate input-impedance matching or without otherwise deteriorating the performance. For example, it is possible to increase the input impedance to some extent by increasing the emitter inductance, but this increases the die area and, in practice, makes it difficult to obtain enough voltage gain from the amplifier. On the other hand, the impedance level could be increased by an external impedance transformation network, but this would complicate the design and increase the cost. In addition, the use of a high-Q off-chip impedance transformation network would make the input matching very sensitive to component variations. On the contrary, by employing only series base inductance for the matching, the Q-value of the input network is moderate and the matching is very tolerant against component variations.

It is concluded that the parallel package parasitic capacitance C_p has a large effect on the properties of the LNA, for example,

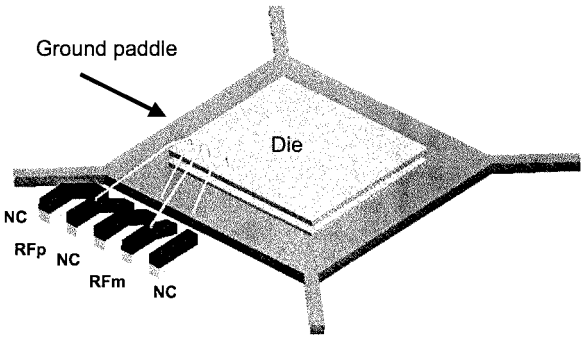

Fig. 7. Bonding arrangement of LNA differential input signal pins "RFp" and "RFm."

in the sense that it drastically lowers the input impedance of the amplifier. However, by simply accepting this lower impedance level and by using a transformer with a lower impedance-transformation ratio, the amplifier performance in terms of NF and power gain is not deteriorated by the package parasitics. On the other hand, if the input impedance of the packaged amplifier has to be increased to be much larger than a few tens of ohms, practical implementation problems will arise, as described above.

IV. LNA Implementation

Based on the results of the LNA analysis, an inductively degenerated common-emitter LNA was designed by using a 0.35-μm SiGe BiCMOS technology. The LNA is a part of the RF front-end of the direct conversion global positioning system (GPS) receiver operating at 1.575 GHz [15]. The RF front-end consists of an LNA, I and Q mixers, LO buffers, a divide-by-two quadrature generator, and a double-frequency VCO. The front-end is mounted in a quad flat nonleaded (QFN) package. The preselection filter with single-ended input and balanced output transforms the single-ended signal differential for the LNA, thus, omitting the need for an additional balun. The input and output impedances of the filter are both 50 Ω. The mixers are implemented as modified Gilbert cells with resistively degenerated common-emitter RF input stages.

Fig. 7 illustrates the bonding arrangement of the LNA differential input signal pins denoted as "RFp" and "RFm." In order to improve the isolation and to reduce the parallel capacitance between each signal pin and ground, the adjacent pins of the input signals on the lead-frame side were left unconnected ("NC"). Moreover, on the die side, the adjacent ground pads of input signals were directly down-bonded to the ground plate. These are the LNA bias ground and the LNA isolation guard ring, respectively. These actions were carried out in order to ensure that the package parasitic capacitance C_p does not become too large. Namely, if C_p is much larger compared to the input device C_π, it becomes difficult to design the input impedance to be even 25 Ω single ended, employing only series base inductance and, eventually, an off-chip matching network must be used.

The package model used in simulations for the LNA input was presented in Fig. 3(a) and it includes the pins shown in Fig. 7. The rest of the package pins (not shown in Fig. 7) have a negligible effect on the front-end performance.

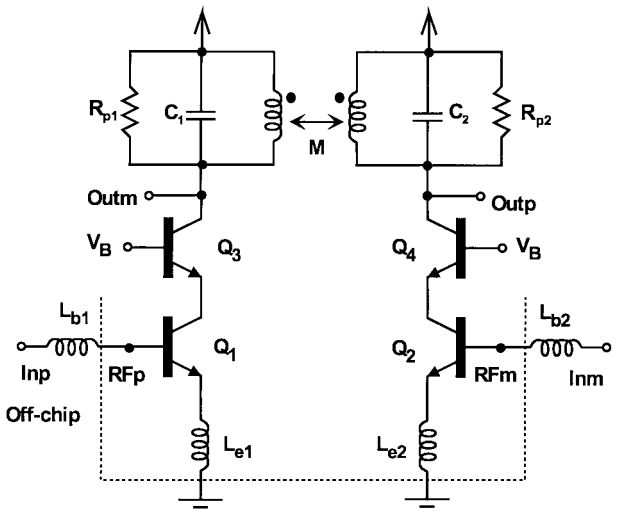

Fig. 8. Schematic of the LNA.

The schematic of the balanced LNA excluding the biasing details is shown in Fig. 8. The amplifier is biased with the proportional-to-absolute temperature (PTAT) base current driven through 20 kΩ resistors used to isolate the bias circuit from the signal path. The LNA and mixers are ac coupled with 4-pF capacitors. The mixers present only a small capacitive load for the LNA.

The sizes of the input devices Q_1 and Q_2 are selected to be a $4\times$ minimum size in order to ensure that the contribution of the r_b to the LNA NF is negligible. Here, the resulted r_b is only approximately 5 Ω. The devices Q_1 and Q_2 are biased at the collector current of 1.1 mA each. Hence, according to (7), the required emitter inductance to realize a single-ended input impedance in the order of 25 Ω is approximately 1.1 nH. In order to resonate the input impedance at 1.575 GHz, the base inductors of 8.2 nH are needed [see (6)]. The base inductors are the only external components of the amplifier.

For the designed LNA, $R_{lb} = 2.2\ \Omega$, $r_b = 5.0\ \Omega$, $R_s = 25\ \Omega$, $k = 0.5$, $I_c = 1.1$ mA, $g_m = 43$ mS, $\beta_0 = 88$, $f_0 = 1.575$ GHz, $C_\pi = 575$ fF, and $R_L = 80\ \Omega$. Substituting data into (12) gives

$$\mathrm{NF} = 1 + \frac{2.20}{25} + \frac{1.25}{25} + \frac{2.58}{25} + \frac{1.02}{25} + \frac{2.12}{25} \approx 1.36\ \mathrm{dB}. \tag{19}$$

Simulations predict 1.54 dB with cascode transistors and bias resistors both contributing approximately 0.1 dB. The largest contributions in this case are seen to be the base shot noise $\overline{i_b^2}$ of the device, the series resistor R_{lb} of the base inductor L_b, and the equivalent parallel load resistance R_L, respectively. The noise contributions of the cascode devices are minimized by using the minimum area devices because the capacitances at their emitters are then minimized [16].

A resonator load peeks the gain of the amplifier at 1.575 GHz. The load comprises a 7-nH differential inductor resonating with the parallel capacitance of 0.95 pF, realized with $C_1 = C_2 = 1.9$ pF and parasitics. The parallel resistors R_{pi} set the LNA voltage gain to 20.5 dB. As the mixer voltage conversion gain was designed to be 5.5 dB, the total RF front-end voltage gain

TABLE I
CALCULATED AND SIMULATED RESULTS OF THE LNA AT A RESONANCE FREQUENCY OF 1.575 GHz

Parameter	Eq.	Calc.	Sim.	Unit
Differential R_{in}	(7)	42.8	44.8	Ω
Input stage G_m	(11)	154	146	mS
Voltage gain	(4)	21.8	20.5	dB
Noise figure	(12)	1.36	1.54	dB

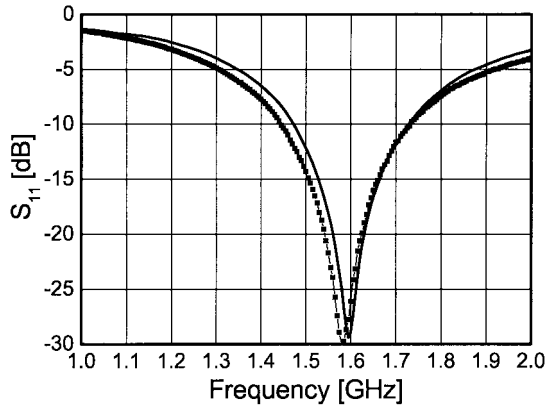

Fig. 9. Measured and simulated (solid line) LNA input-impedance matching.

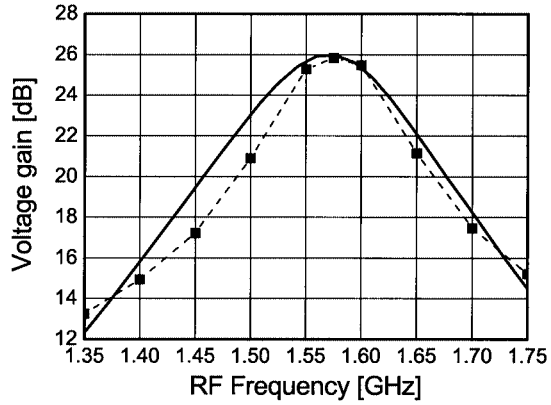

Fig. 10. Measured and simulated (solid line) RF front-end voltage gain.

is approximately 26 dB. With this gain distribution, the double-sideband (DSB) NF of 2.7 dB was obtained for the whole RF front-end with sufficient linearity and low power consumption.

A summary of the calculated versus simulated results of the designed LNA is given in Table I. As seen, the calculated values are very close to the simulated ones. Therefore, the formulas derived in Section III can be applied in the initial design phase to get a first estimate of the LNA performance without the need for running several circuit simulations. The difference of 1.3 dB between the calculated and simulated voltage gain is mostly due to the parasitic capacitance at the emitter of cascode transistors. This capacitance draws part of the output signal current of the LNA input stage and, therefore, lowers the voltage gain of the amplifier.

The simulated and measured LNA scattering parameter S_{11} and RF front-end voltage conversion gain are plotted in Figs. 9 and 10, respectively. The front-end voltage conversion gain is plotted at the fixed LO frequency of 1.575 GHz. To relax the linearity requirements of the baseband block following the RF front-end, the output of the mixer consist of a first-order *RC* low-pass filter. The effect of this pole is clearly seen in Fig. 10.

TABLE II
SIMULATED AND EXPERIMENTAL RESULTS OF THE RF FRONT-END AT 1.575 GHz

Parameter	Sim.	Meas.	Unit
S_{11} (balanced 50 Ω)	-29	≤ -25	dB
Voltage gain	26.0	25.8	dB
DSB-NF	2.3	2.7	dB
IIP3 (in-band)	-16.5	-14.5	dBm
Current consumption	7.4	9.0	mA

The most relevant measurement and simulated results of the front-end are summarized in Table II. The measurement results are seen to be very similar with simulation results. The reported current consumption includes an LNA (2.7 mA) and I and Q mixers (6.3 mA). The current consumption of 9.0 mA is higher than the expected 7.4 mA because the PTAT bias current used to bias the front-end was generated on-chip and this reference current varies with the sheet resistance of an integrated polysilicon resistor.

V. CONCLUSIONS

In this paper, the effects of packaging on the input matching, input stage transconductance, NF, and voltage gain of the inductively degenerated common-emitter LNA have been examined. By applying the derived formulas, the LNA performance can be immediately estimated and optimized without running several circuit simulations, provided that few transistor parameters are available. In addition, the guidelines for the LNA design have been obtained from the given equations. It is concluded that, in the presence of parasitic package capacitance C_p at the transistor base, it can be difficult to design the input-impedance level of the amplifier to be as large as a 100-Ω differential. By simply choosing a smaller impedance level like 50 Ω in this study, the inductively degenerated common-emitter LNA can be realized with better input-impedance matching and by using a smaller die area without any loss in the amplifier performance. Since the simulated and measured results of the implemented RF front-end agree, and the calculated and simulated LNA performance are similar, the results of the LNA analysis are found to be implicitly consistent with the measured performance.

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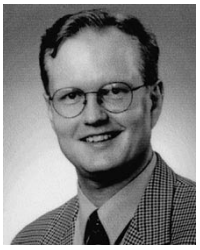

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